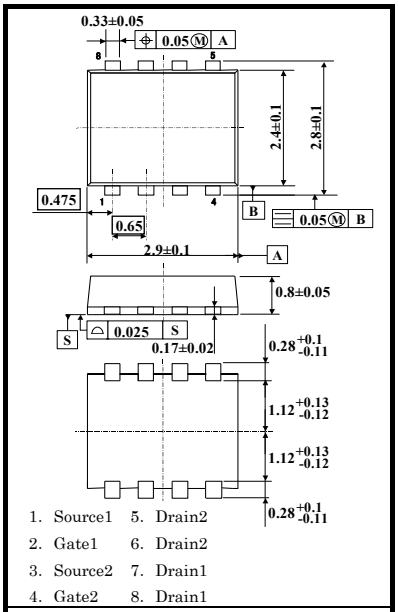
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOS Ⅳ)

TPCP8204

Portable Equipment Applications
Motor Drive Applications

- Small footprint due to small and thin package
- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 38 mΩ (typ.) (VGS=10V)
- High forward transfer admittance: $|Y_{fs}|$ = 8 S (typ.)
- Low leakage current: I_{DSS} = 10 μA (V_{DS} = 30 V)
- Enhancement mode: V_{th} = 1.3 to 2.5 V (V_{DS} = 10 V, I_D = 1mA)

Unit: mm



JEDEC	―
JEITA	―
TOSHIBA	2-3V1G

Weight: 0.017 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

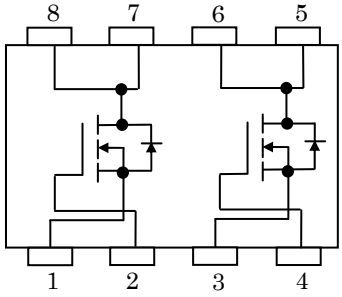
Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	30	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	4.2	A
	Pulse (Note 1)	I_{DP}	16.8	
Drain power dissipation (t = 5 s) (Note 2a)	Single-device operation (Note 3a)	$P_{D\ (1)}$	1.48	W
	Single-device value at dual operation (Note 3b)	$P_{D\ (2)}$	1.23	
Drain power dissipation (t = 5 s) (Note 2b)	Single-device operation (Note 3a)	$P_{D\ (1)}$	0.58	
	Single-device value at dual operation (Note 3b)	$P_{D\ (2)}$	0.36	
Single pulse avalanche energy (Note 4)		E_{AS}	2.86	mJ
Avalanche current		I_{AR}	2.1	A
Repetitive avalanche energy Single-device value at dual operation (Note 2a, 3b, 5)		E_{AR}	0.009	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note: For Notes 1 to 6, refer to the next page.

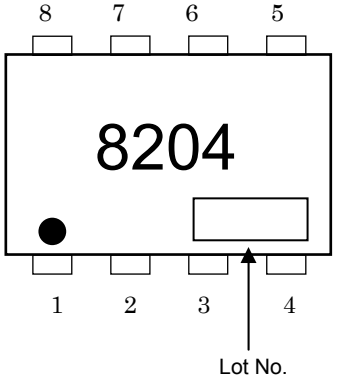
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with caution.

Circuit Configuration



Marking (Note 6)

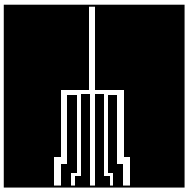


Thermal Characteristics

Characteristics		Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 5 s) (Note 2a)	Single-device operation (Note 3a)	$R_{th\ (ch\text{-}a)\ (1)}$	84.5	°C/W
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch\text{-}a)\ (2)}$	101.6	
Thermal resistance, channel to ambient (t = 5 s) (Note 2b)	Single-device operation (Note 3a)	$R_{th\ (ch\text{-}a)\ (1)}$	215.5	°C/W
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch\text{-}a)\ (2)}$	347.2	

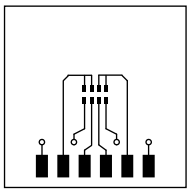
Note 1: The channel temperature should not exceed 150°C during use.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

(a)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

(b)

Note 3: a) The power dissipation and thermal resistance values shown are for a single device. (During single-device operation, power is only applied to one device.)

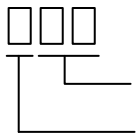
b) The power dissipation and thermal resistance values shown are for a single device. (During dual operation, power is evenly applied to both devices.)

Note 4: V_{DD} = 24 V, T_{ch} = 25°C (initial), L = 0.5 mH, R_G = 25 Ω, I_{AR} = 2.1 A

Note 5: Repetitive rating: pulse width limited by maximum channel temperature.

Note 6: ● on the lower left of the marking indicates Pin 1.

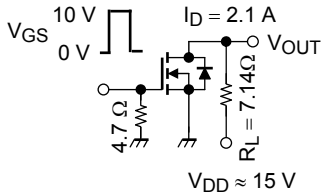
※ Weekly code (3 digits):



Week of manufacture
(01 for the first week of the year, continuing up to 52 or 53)

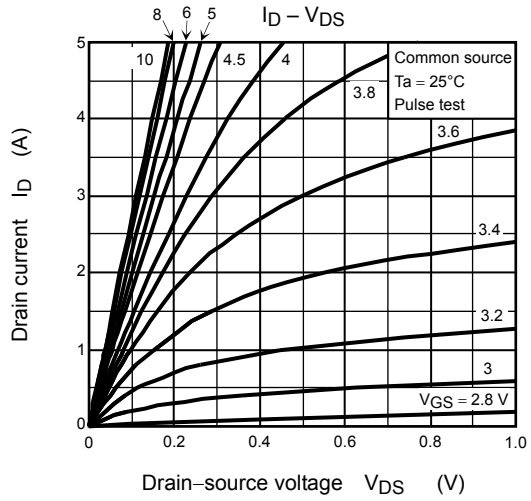
Year of manufacture
(The last digit of the calendar year)

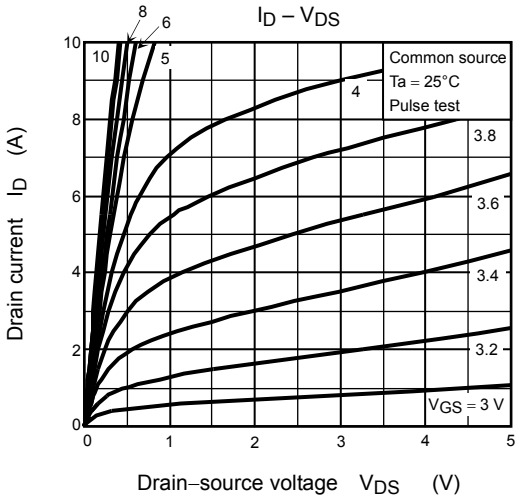
Electrical Characteristics (Ta = 25°C)

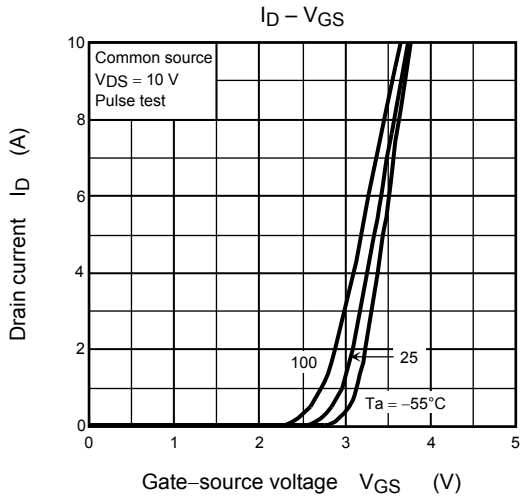
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±100	nA
Drain cut-off current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	30	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = −20 V	10	—	—	
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	1.3	—	2.5	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 4.5 V, I_D = 2.1 A	—	58	77	mΩ
			V_{GS} = 10 V, I_D = 2.1 A	—	38	50	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 2.1 A	4	8	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	190	—	pF
Reverse transfer capacitance		C_{rss}		—	45	—	
Output capacitance		C_{oss}		—	65	—	
Switching time	Rise time	t_r	 Duty ≤ 1%, t_w = 10 μs	—	4.5	—	ns
	Turn-on time	t_{on}		—	9.0	—	
	Fall time	t_f		—	3.0	—	
	Turn-off time	t_{off}		—	12.0	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ 24 V, V_{GS} = 10 V, I_D = 4.2 A	—	4.6	—	nC
Gate-source charge 1		Q_{gs1}		—	0.7	—	
Gate-drain (“miller”) charge		Q_{gd}		—	1.4	—	

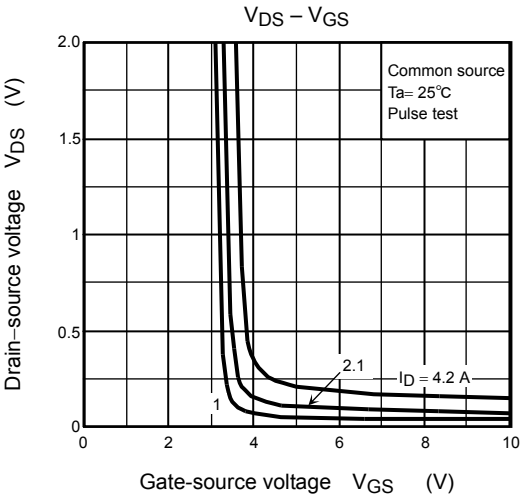
Source-Drain Ratings and Characteristics (Ta = 25°C)

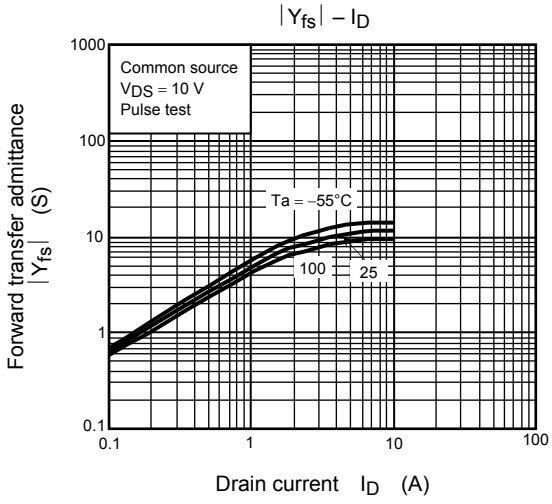
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	16.8	A
Forward voltage (diode)		V_{DSF}	I_{DR} = 4.2 A, V_{GS} = 0 V	—	—	−1.2	V

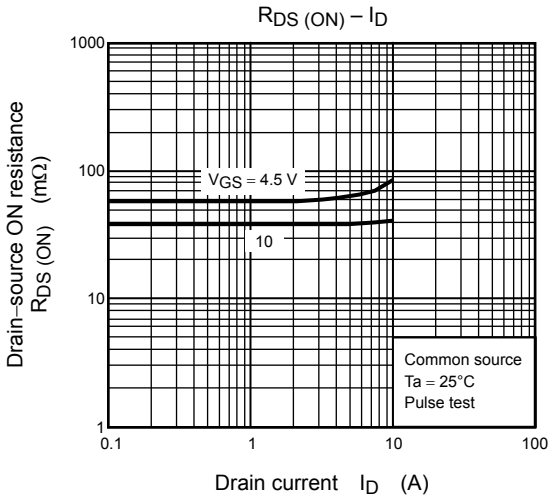

$I_D - V_{DS}$
Common source
Ta = 25°C
Pulse test
8
6
5
10
4.5
4
3.8
3.6
3.4
3.2
3
V_{GS} = 2.8 V
Drain current I_D (A)
Drain–source voltage V_{DS} (V)


$I_D - V_{DS}$
Common source
Ta = 25°C
Pulse test
8
6
10
5
4
3.8
3.6
3.4
3.2
V_{GS} = 3 V
Drain current I_D (A)
Drain–source voltage V_{DS} (V)

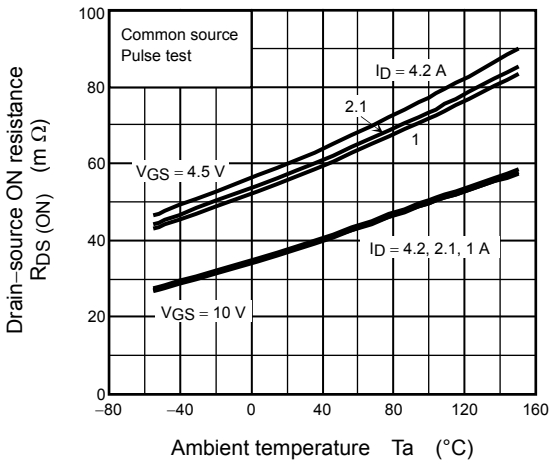

$I_D - V_{GS}$
Common source
V_{DS} = 10 V
Pulse test
100
25
Ta = −55°C
Drain current I_D (A)
Gate–source voltage V_{GS} (V)


$V_{DS} - V_{GS}$
Common source
Ta= 25°C
Pulse test
2.1
I_D = 4.2 A
1
Drain–source voltage V_{DS} (V)
Gate-source voltage V_{GS} (V)

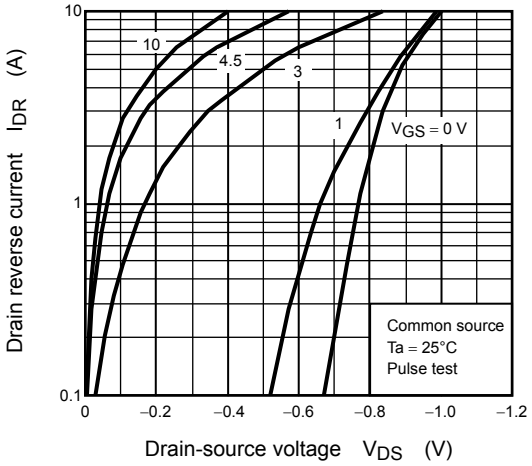

$|Y_{fs}| - I_D$
Common source
V_{DS} = 10 V
Pulse test
Ta = −55°C
100
25
Forward transfer admittance $|Y_{fs}|$ (S)
Drain current I_D (A)


$R_{DS\ (ON)} - I_D$
V_{GS} = 4.5 V
10
Common source
Ta = 25°C
Pulse test
Drain–source ON resistance $R_{DS\ (ON)}$ (mΩ)
Drain current I_D (A)

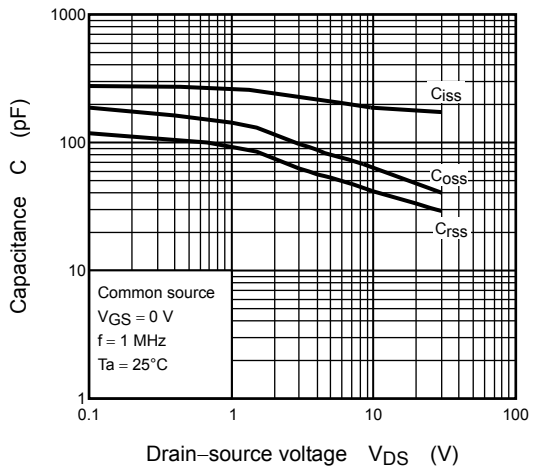
$R_{DS\ (ON)}$ – Ta



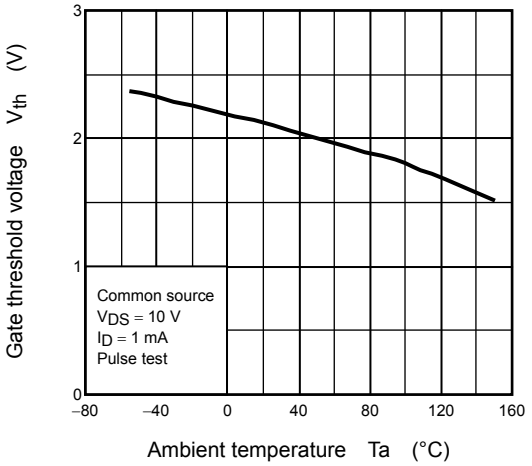
I_{DR} – V_{DS}



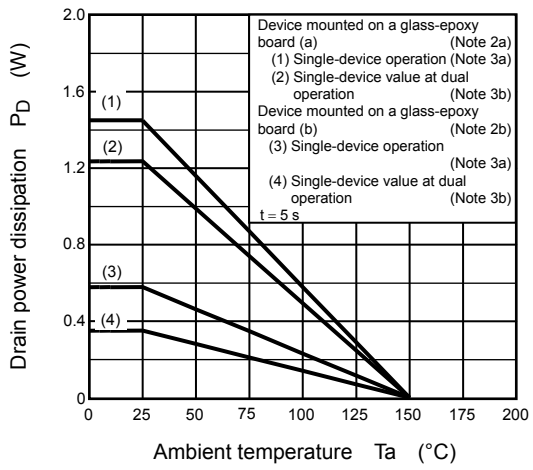
Capacitance – V_{DS}



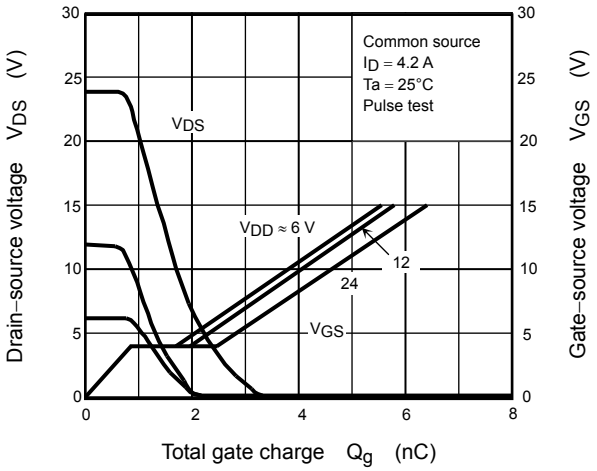
V_{th} – Ta



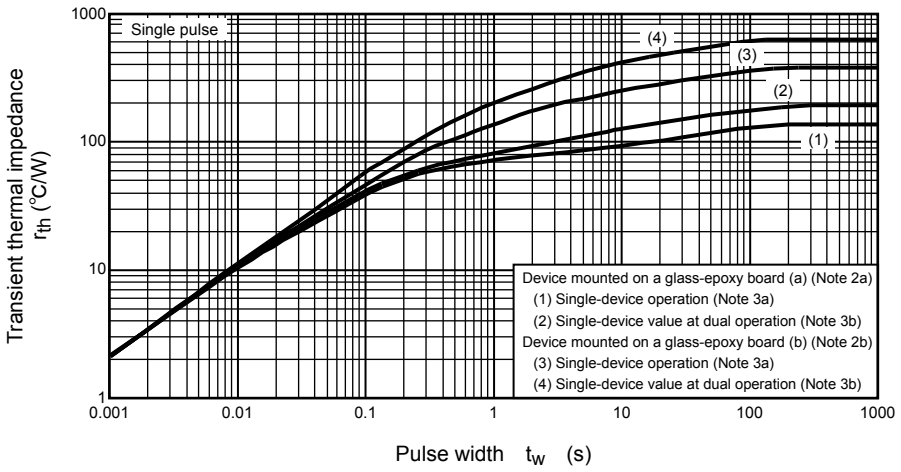
P_D – Ta



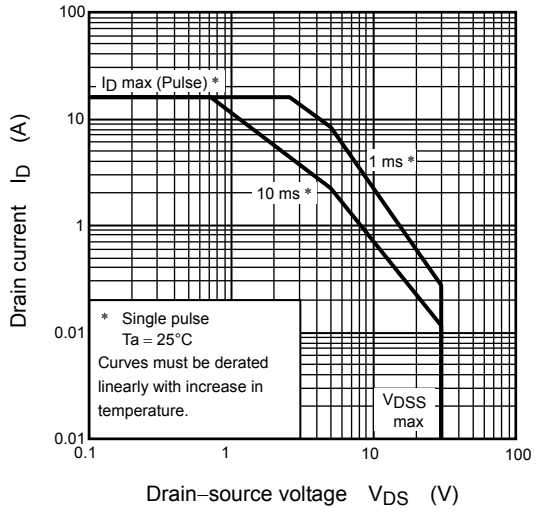
Dynamic input/output characteristics



$r_{th} - t_w$



Safe operating area



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